IN THE CLAIMS:

1. (Currently Amended) A method of creating a symmetrical signal from a pair of pulse width modulated signals, comprising the steps of:

applying one of the pair of pulse width modulated signals both to a set input of a latch circuit and to a delay circuit;

applying the other of the pair of pulse width modulated signals to a reset input of the latch circuit, wherein both of the pair of pulse width modulated signals have substantially constant and equidistant start transition times; and

obtaining a constant width drive signal from the output of said latch circuit.

2. (Currently Amended) Apparatus for generating a symmetrical signal from a complementary pair of pulse width modulated signals, comprising:

a first pulse width modulated control signal supplying means connected at least to a delay circuit;

a second pulse width modulated control signal supplying means, wherein both of the pair of pulse width modulated control signal supplying means have substantially constant and equidistant start transition times;

a toggle circuit, connected to said first and second control signal supplying means, the toggle circuit supplying a first output drive signal level upon detecting a given characteristic of a first pulse width modulated control signal received from said first supplying means and supplying a second output drive signal level upon detecting said given characteristic of a second pulse width modulated control signal received from said second supplying means, whereby substantially symmetrical first and second output drive signals are generated from said toggle circuit.

3. (Previously Presented) A method of generating a pulse width modulated signal and a symmetrical signal from a pair of pulse width modulated signals, comprising the steps of:

applying one of the pair of first pulse width modulated signals to a set input of a latch circuit as well as to a turn-on delay circuit wherein the turn-on delay is such that an output voltage transition of the turn-on delay circuit coincides with an output voltage transition of the latch circuit;

applying the other of the pair of first pulse width modulated signals to a reset input of the latch circuit;

obtaining a constant pulse width drive signal from the output of said latch circuit; and

obtaining a second pulse width modulated drive signal from the output of the turn-on delay circuit.

4. (Previously Presented) A method of generating a pulse width modulated signal and a symmetrical signal from a pair of pulse width modulated signals, comprising the steps of:

applying one of the pair of first pulse width modulated signals to a toggle circuit as well as to a delayed turn-on drive circuit wherein the turn-on delay is such that an output voltage transition of the delayed turn-on circuit coincides with an output voltage transition of the toggle circuit;

applying the other of the pair of first pulse width modulated signals to said toggle circuit;

obtaining a symmetrical drive signal from the output of said toggle circuit; and

obtaining a second pulse width modulated drive signal from the output of the delayed turn-on circuit.

5. (Previously Presented) A method of generating drive signals from a pair of pulse width modulated input control signals, comprising the steps of:

applying both of a pair of pulse width modulated control signals to a first drive circuit;

toggling said first drive circuit between predetermined output drive signal voltage levels upon detection of a given transition characteristic of each of the pair of pulse width modulated input control signals; and

delaying the application of one of said pair of pulse width modulated control signals to a second drive circuit whereby an output voltage transition of the second circuit coincides with an output voltage transition of the toggled drive circuit.

6. (Original) The method of claim 5, comprising the additional steps of:

applying said pair of pulse width modulated control signals to a third drive circuit for toggling said third drive circuit whereby a drive signal complementary to the output drive signal of said first drive circuit is generated; and

delaying the application of the other of said pair of pulse width modulated control signals to a fourth drive circuit whereby an output voltage transition of said fourth circuit coincides with an output voltage transition of one of the toggled drive circuits.

7. (Original) Apparatus for generating a pulse width modulated signal and a symmetrical signal, comprising:

first and second pulse width modulated signal supplying means;

a latch circuit, connected to said first and second signal supplying means, the latch circuit changing states upon detection of a given characteristic of received pulse width modulated signals at set and reset inputs thereof; and

a delayed turn-on circuit, connected to said first signal supplying means, the turn-on circuit receiving the pulse width modulated signal therefrom, the turn-on delay causing an output voltage transition of the delayed turn-on circuit to coincide with an output voltage transition of the latch circuit.

8. (Original) Apparatus for generating a pulse width modulated signal and a symmetrical signal, comprising:

first and second pulse width modulated signal supplying means;

a toggle circuit, connected to said first and second signal supplying means, the toggle circuit toggling between first output drive signal states upon detection of a given characteristic of received pulse width modulated signals; and

a delayed turn-on circuit, connected to said first signal supplying means, the delayed turn-on circuit receiving a pulse width modulated signal therefrom, the turn-on delay causing a voltage transition of a generated second output drive signal of the turn-on delay circuit to coincide with an output voltage transition of the first drive signal.

9. (Original) Apparatus as claimed in claim 8, comprising in addition:

an additional toggle circuit, connected to said first and second signal supplying means, the additional toggle circuit generating an output drive signal complementary to the first drive signal; and

an additional delayed turn-on circuit, connected to said first signal supplying means, the additional delayed turn-on circuit generating a fourth output drive signal complementary to said second output drive signal.